AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:
a processor core;
a configurable logic block coupled to the processor core;
a configurable peripheral device; and
a bus connecting said processor core and said configurable peripheral device.

2. (Original) The integrated circuit of claim 1 wherein said peripheral device is a universal asynchronous receiver transmitter (UART).

3. (Original) The integrated circuit of claim 2 wherein said UART has a fixed baud rate.

4. (Original) The integrated circuit of claim 1 wherein said processor core, said configurable peripheral device and said bus are implemented on a field programmable gate array.

5. (Original) The integrated circuit of claim 1 wherein said peripheral device is a flash memory controller.

6. (Currently Amended) A system allowing a user to select peripheral devices in a programmable logic device, comprising:
a menu system allowing said user to select one of a plurality of peripheral devices; and
~~an integrated circuit~~ the programmable logic device comprising:
a processor core;
a configurable peripheral device corresponding to said one peripheral device selected using said menu system; and
a bus connecting said processor core and said configurable peripheral device.

Claims 7-9. (Canceled)

10. (New) The system of claim 6 wherein said user selectable options comprise at least one of a UART peripheral selector, an Ethernet peripheral selector and a flash memory peripheral selector.

11. (New) The system of claim 10 wherein said user selectable options comprise at least one data width size selector responsive to selection of said flash memory peripheral selector.

12. (New) The system of claim 10 wherein said user selectable options comprise an error correction selector responsive to selection of said flash memory peripheral selector.

13. (New) The system of claim 12 wherein said user selectable options comprise at least one error correction code selector responsive to selection of said error correction selector.

14. (New) The integrated circuit of claim 1 further comprising a user interface having computer displayed user selectable options for configuring said configurable peripheral device, said processor core responsive to selection of at least one of the user selectable options for configuring said configurable peripheral device, said processor core having access to a hardware design language file for configuring said configurable logic responsive to the selection of the at least one of said user selectable options.